

Computer Organization and Assembly

A course dealing with the fundamentals of computer architecture using case study of MIPS architecture. A methodical discussion of number systems, arithmetic and basic computer organization including: assembly language programming.

Prerequisite

- Digital Logic and Computer Design
- Microprocessors

Text

- *Computer Organization and Design*, David A. Patterson, John L. Hennessy, 3rd ed, The Morgan Kaufmann.

Reference

- *Computer Organization and Architecture*, William Stallings, Prentice Hall.
- *Computer System Architecture*, M. Morris Mano, Prentice Hall.
- *Computer Systems Design and Architecture*, Vincent P. Heuring and Harry F. Jordan, Prentice Hall.

Marking Scheme

Quizzes and Assignments	:	20%
Mid Term	:	40%
Final Term	:	40%

Notes

- Students must work on their assignments independently
- Homework assignment is due in class. No late submissions are accepted
- Identical or almost identical assignments from separate individuals are considered evidence of plagiarism, subject to disciplinary actions
- Open/closed-book examination will be used for both mid-semester and final exam

Instructor Contact

- sns_ee04@yahoo.com

Lectures and Assignments Plan

Week	1st Lecture	2nd Lecture
1	Introduction to Computer Organization	Operands of Computer Hardware
2	Arithmetic and Logical Instructions	Branch Instructions
3	Procedure Calls	Representation of Instructions in Machine Language
4	Representation of Instructions in Machine Language	Byte Operations, 32 bit Immediate Data, Arrays and Pointers
5	Translation of C program into Assembly	Number Systems, Addition and Subtraction
6	Multiplication and Division	Floating Point Numbers
7	Performance Measures	Components of Datapath
8	Single Cycle Implementation of Datapath contd.	Single Cycle Implementation of Datapath contd.
9	Single Cycle Implementation of Datapath contd.	Multicycle implementation of datapath contd.
10	Multicycle implementation of datapath contd.	Multicycle implementation of datapath
11	Midterm Exam	Exam Solution Discussion
12	Control Unit Design	Pipelining and Hazards
13	Data Hazards and Data Forwarding	Branch Hazards
14	Memory Hierarchy and Caches	Caches and Cache Performance
15	Virtual Memory	Virtual Memory
16	Discs, Storage and Buses	Interfacing IO devices